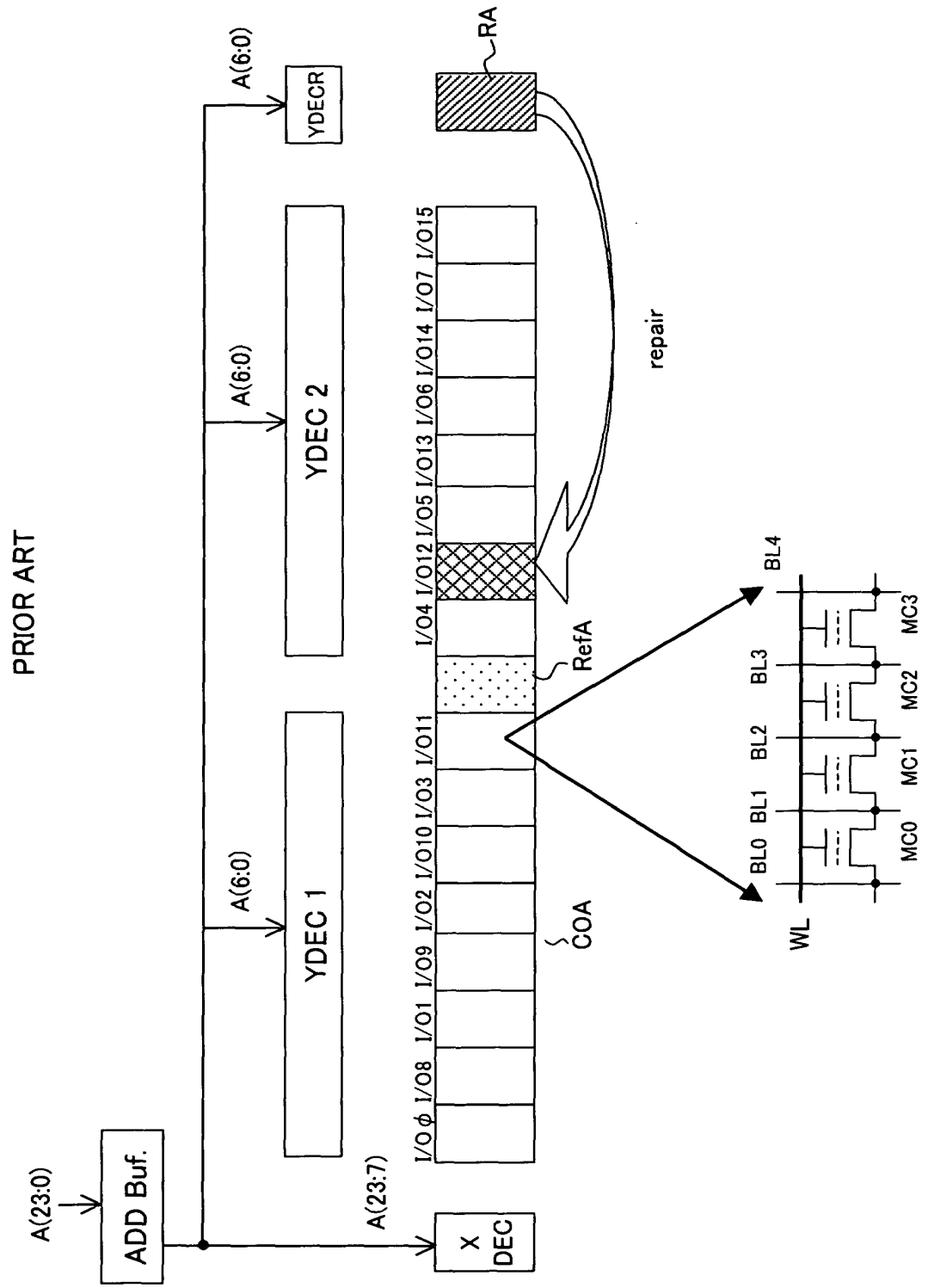
FIG. 1


PRIOR ART
A(23:0)
ADD Buf.
A(6:0)
YDECR
YDEC 2
YDEC 1
A(23:7)
X DEC
RA
repair
RefA
COA
I/O0 I/O8 I/O1 I/O9 I/O2 I/O10 I/O3 I/O11 I/O4 I/O12 I/O5 I/O13 I/O6 I/O14 I/O7 I/O15
BL4
BL3
BL2
BL1
BL0
MC3
MC2
MC1
MC0
WL

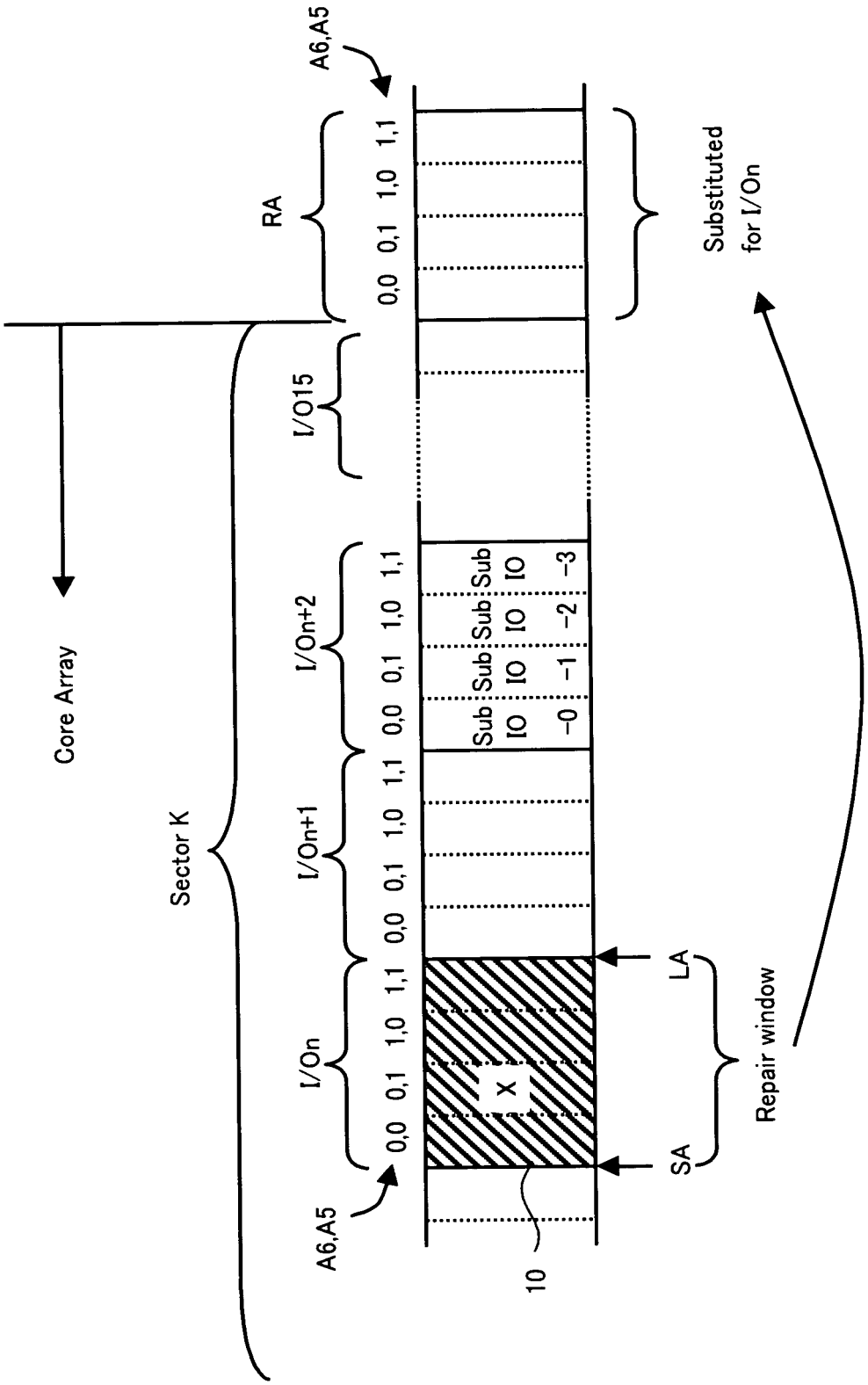
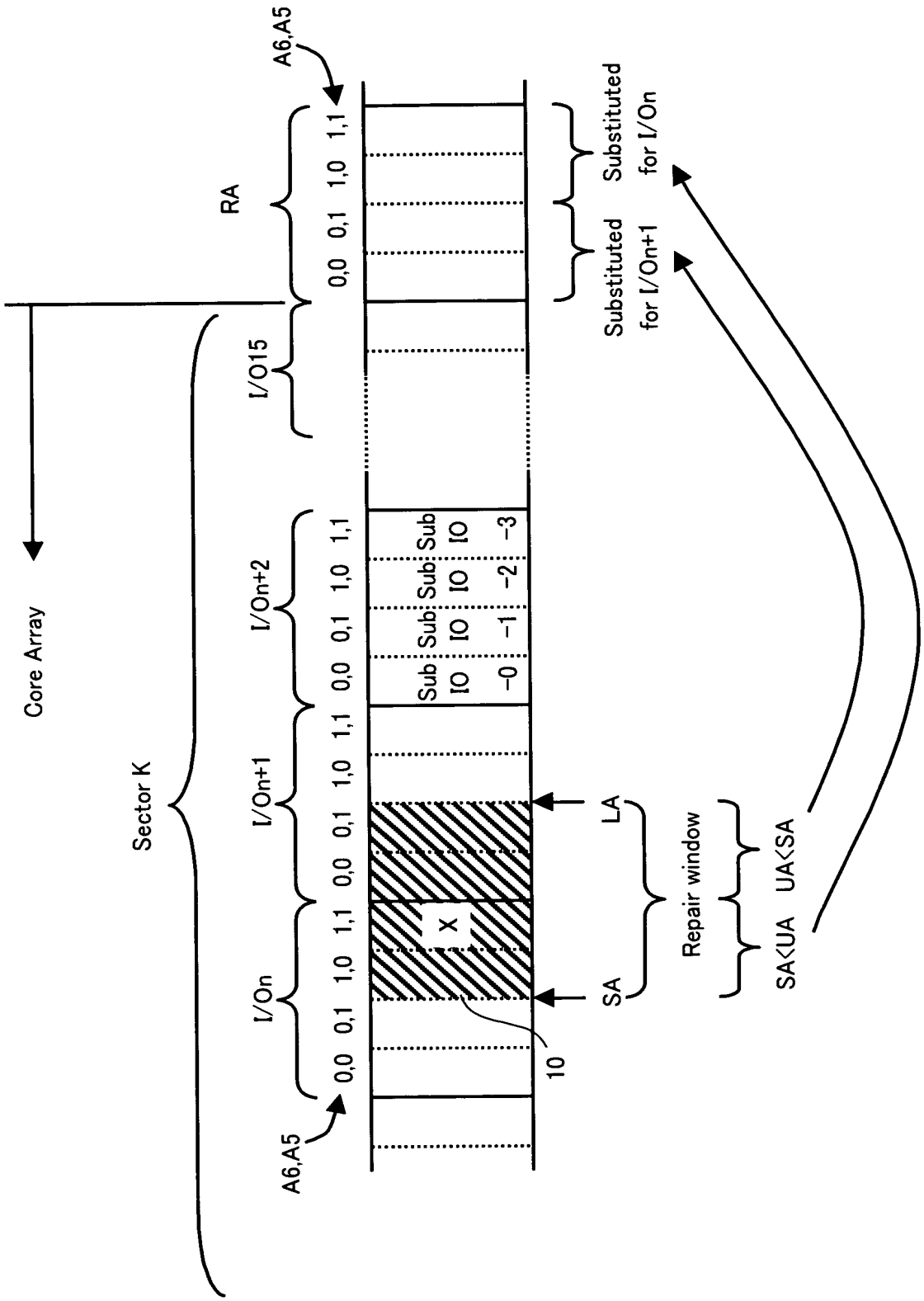

A6,A5
RA
0,0 0,1 1,0 1,1
Substituted
for I/On
I/O15
Core Array
I/On+2
I/On+1
I/On
Sub IO -0
Sub IO -1
Sub IO -2
Sub IO -3
Sector K
0,0 0,1 1,0 1,1
LA
SA
X
Repair window
A6,A5
10

FIG. 2

FIG. 3


A6,A5
RA
I/O15
0,0 0,1 1,0 1,1
Core Array
Sector K
I/On+2
I/On+1
I/On
Sub IO -0
Sub IO -1
Sub IO -2
Sub IO -3
X
10
A6,A5
0,0 0,1 1,0 1,1
LA
SA
Repair window
SA<UA UA<SA
Substituted for I/On+1
Substituted for I/On

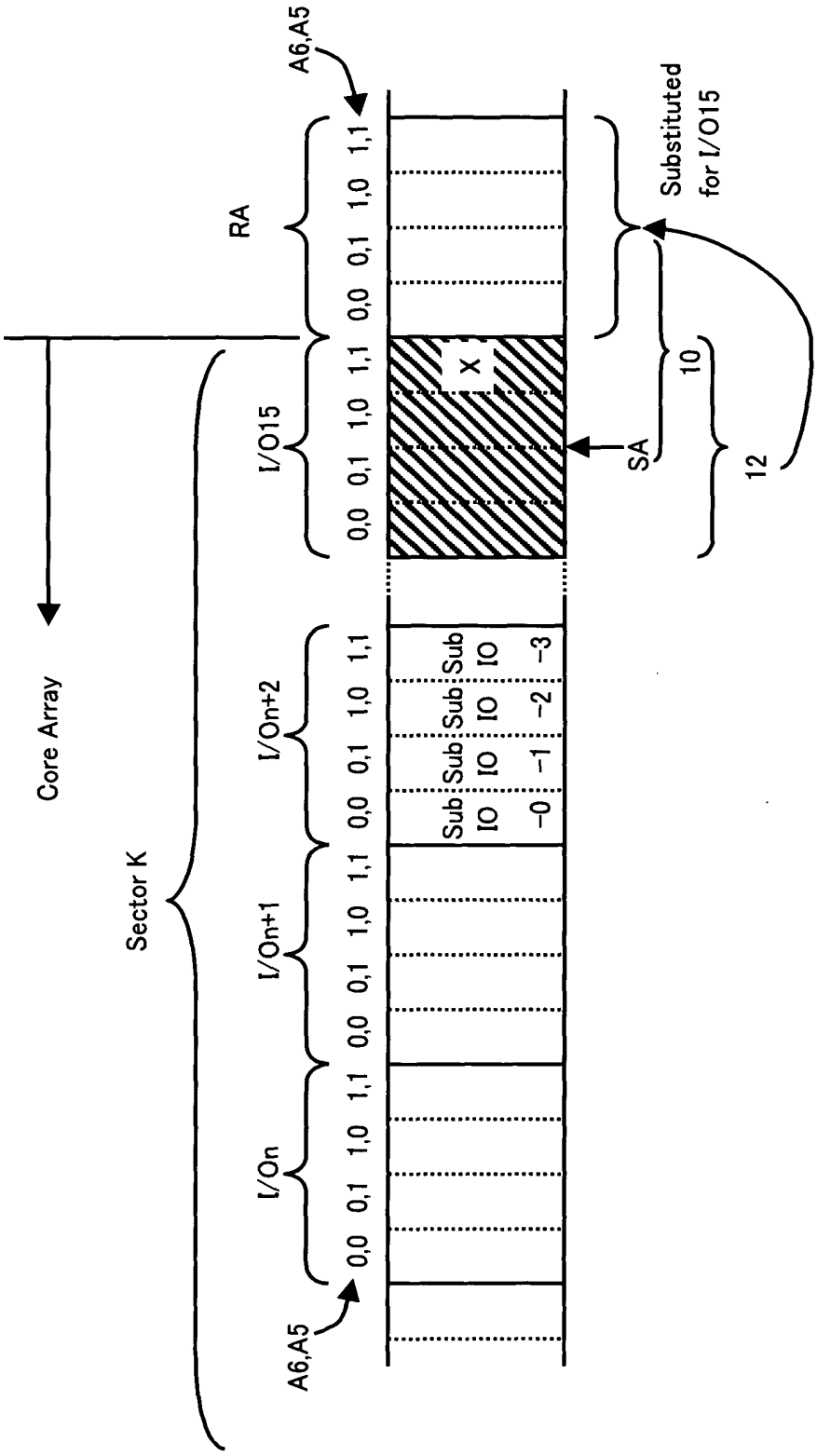

A6,A5
RA
Substituted
for I/O15
Core Array
I/O15
I/On+2
I/On+1
I/On
Sector K
SA
10
12
0,0 0,1 1,0 1,1
Sub IO -0
Sub IO -1
Sub IO -2
Sub IO -3
X

FIG. 4

Title: Semiconductor Memory Enabling Correct Substitution of Redundant Cell Array
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FIG. 5

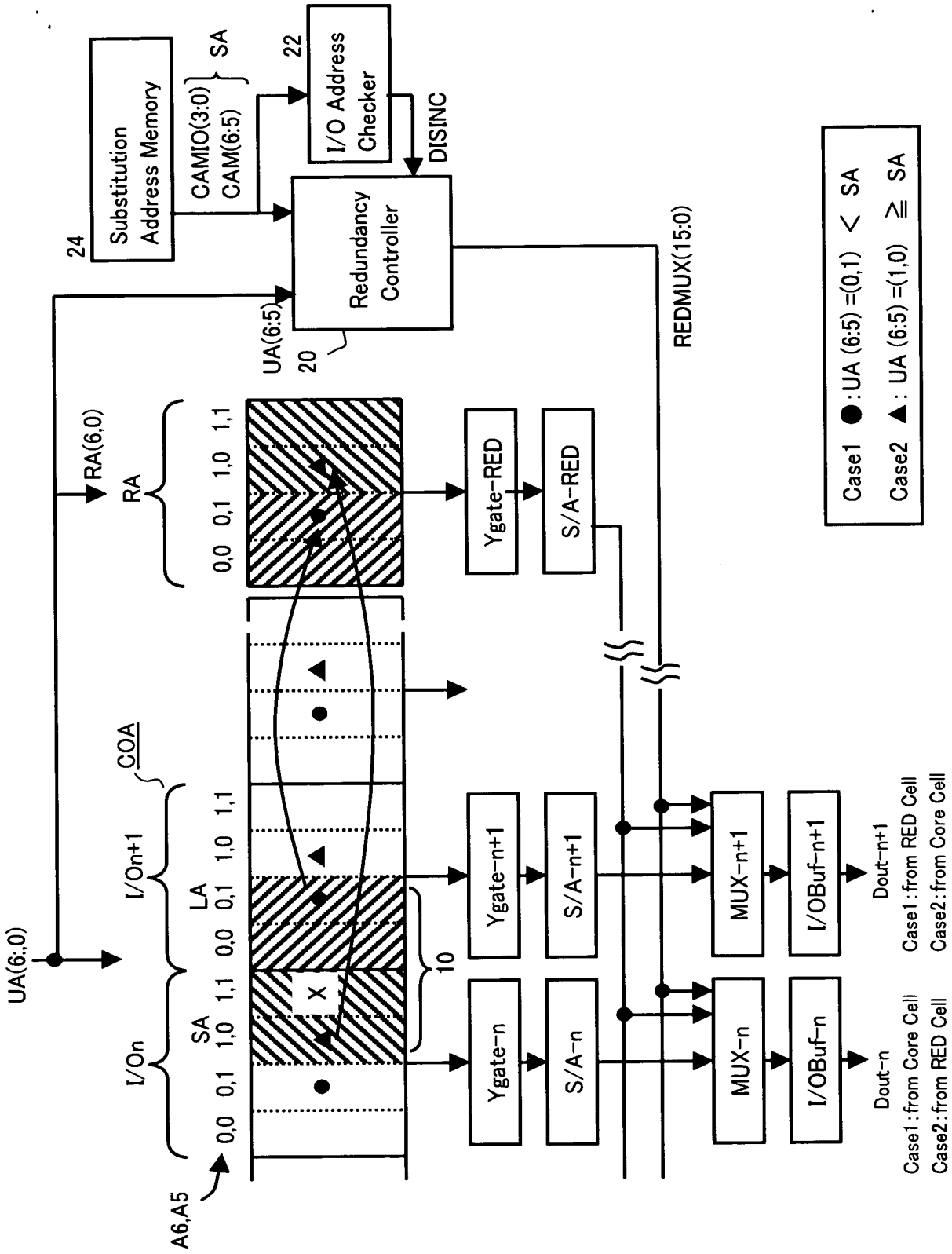


FIG. 6

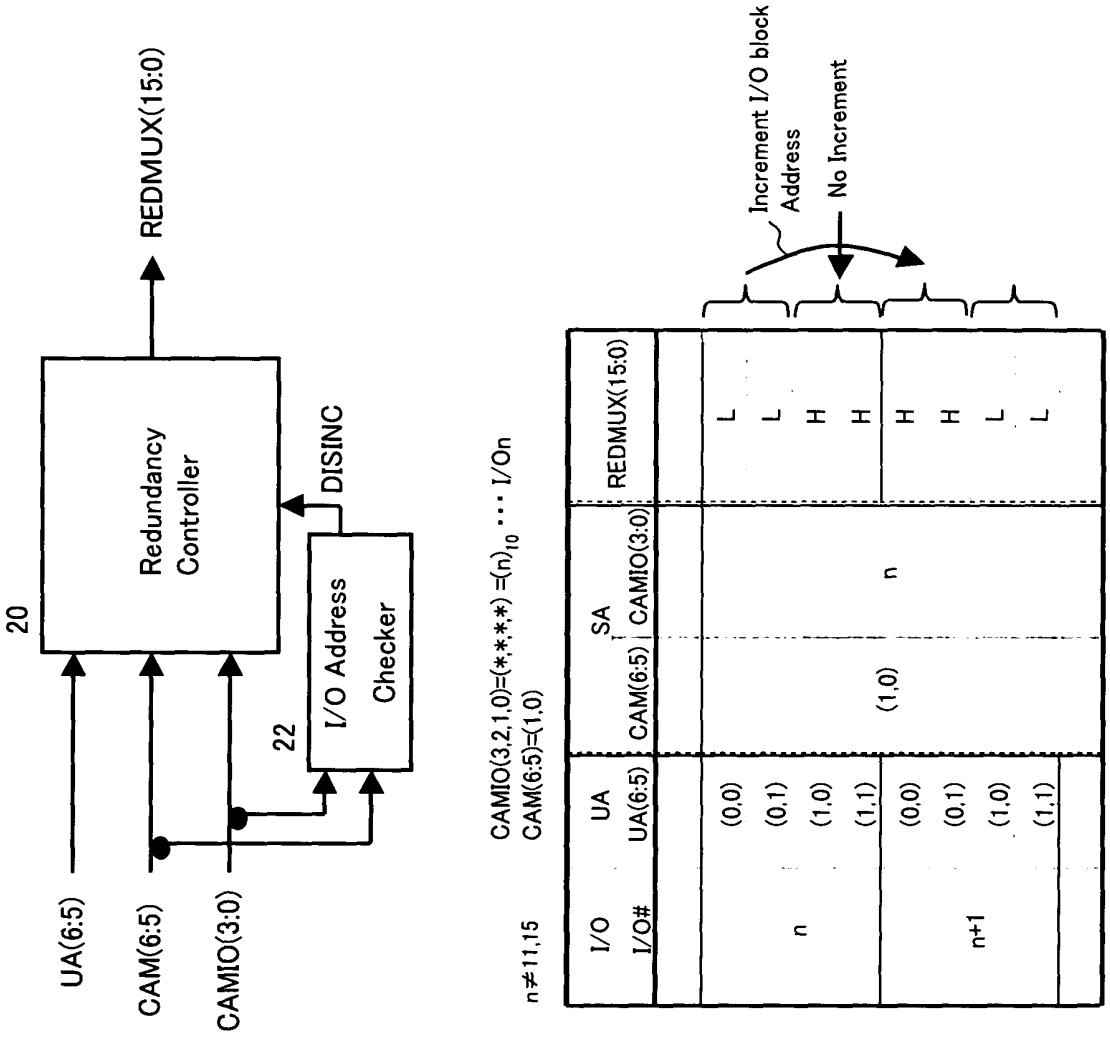

REDMUX(15:0)
20
Redundancy Controller
DISINC
22
I/O Address Checker
UA(6:5)
CAM(6:5)
CAMIO(3:0)
Increment I/O block Address
No Increment
CAMIO(3,2,1,0)=(*,*,*,*) =(n)10 ··· I/On
CAM(6:5)=(1,0)
n≠11,15
I/O
I/O#
UA
UA(6:5)
SA
CAM(6:5)
CAMIO(3:0)
REDMUX(15:0)
n
n+1
(0,0)
(0,1)
(1,0)
(1,1)
L
H

FIG. 7

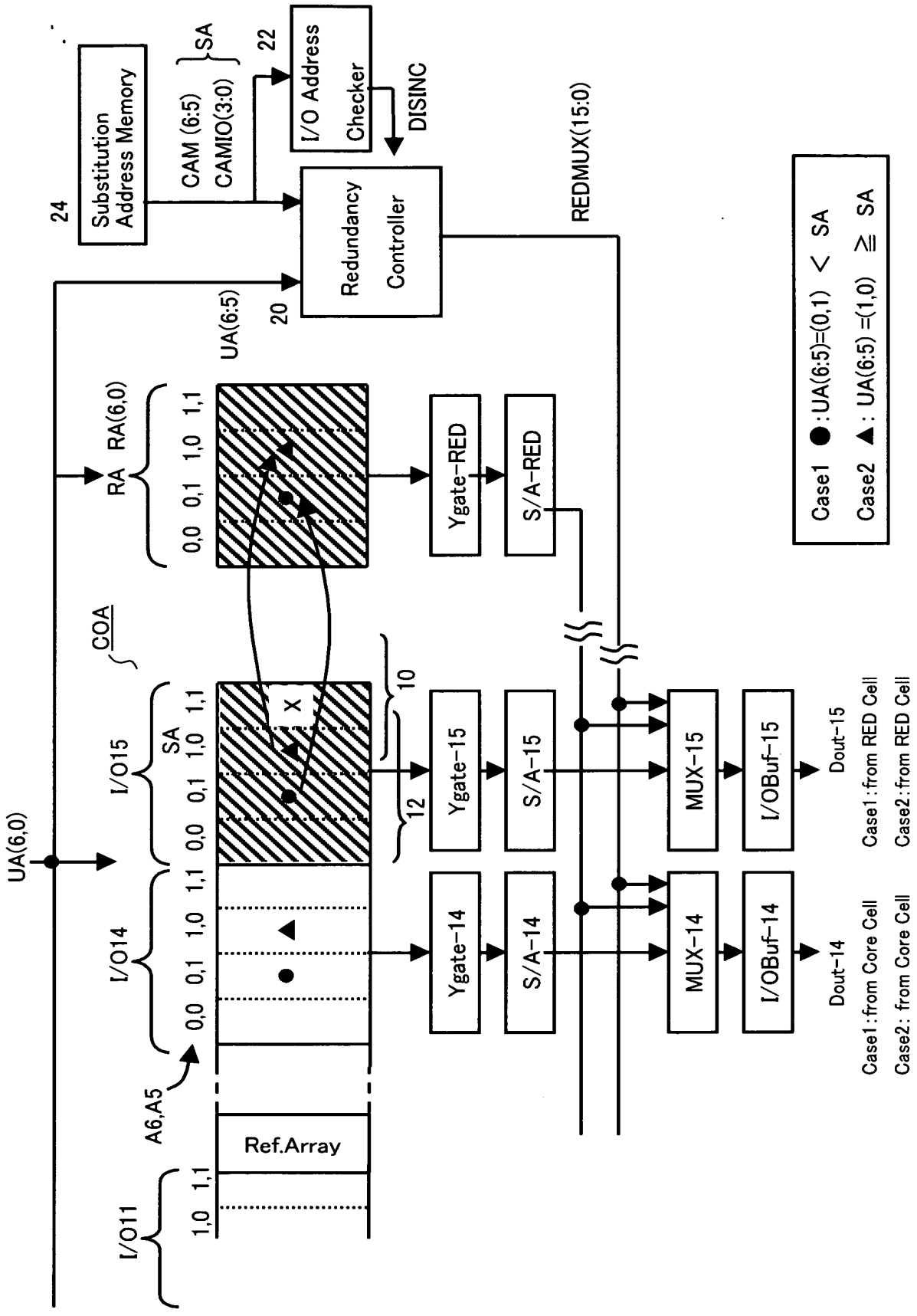
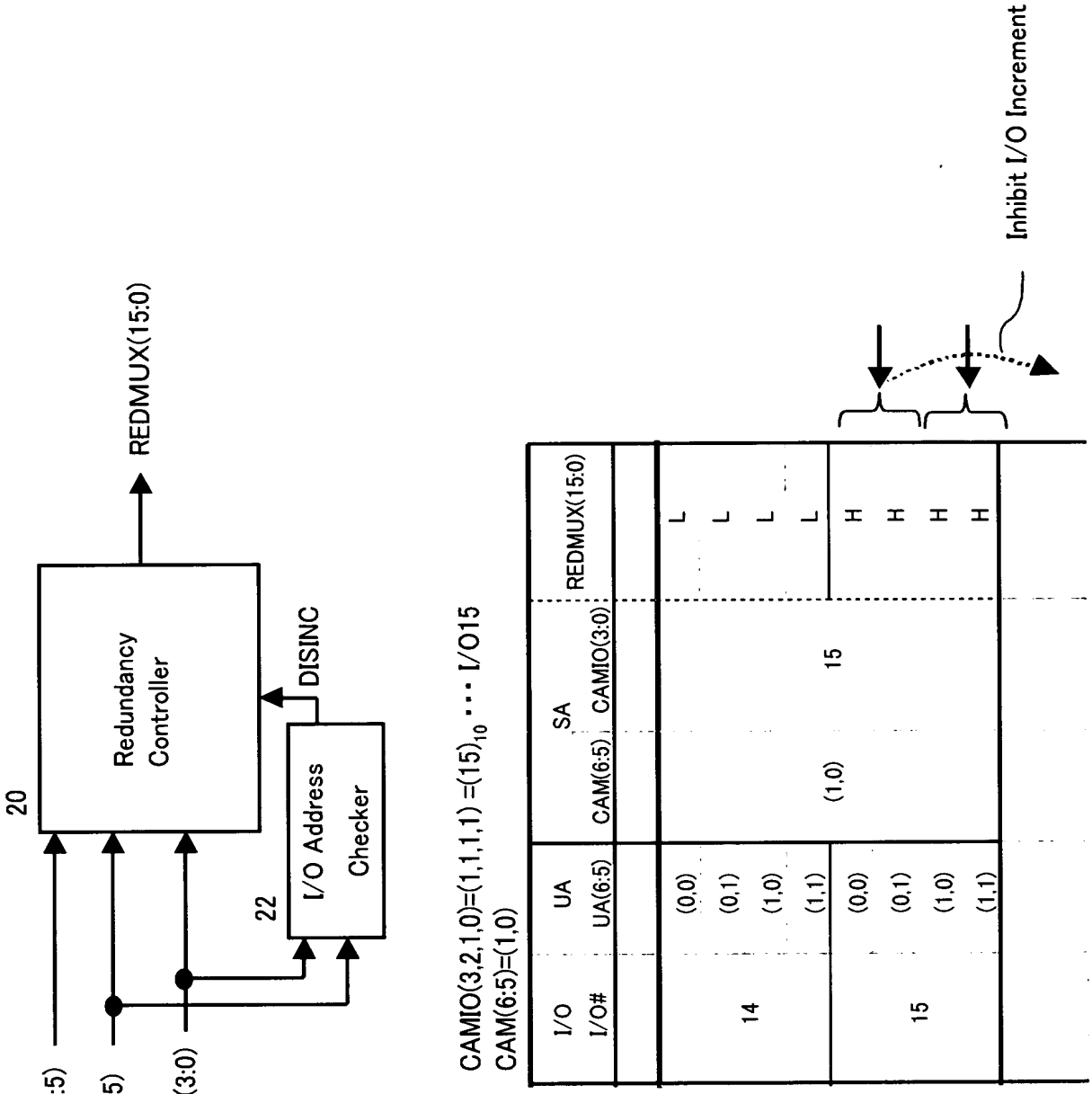

Substitution Address Memory
24
CAM (6:5)
CAMIO(3:0)
SA
22
I/O Address Checker
DISINC
Redundancy Controller
20
UA(6:5)
REDMUX(15:0)
RA
RA(6,0)
0,0 0,1 1,0 1,1
Ygate-RED
S/A-RED
COA
I/O15
I/O14
I/O11
SA
UA(6,0)
A6,A5
Ref.Array
10
12
Ygate-15
S/A-15
MUX-15
I/OBuf-15
Dout-15
Ygate-14
S/A-14
MUX-14
I/OBuf-14
Dout-14
Case1 ●: UA(6:5)=(0,1) < SA
Case2 ▲: UA(6:5) =(1,0) ≧ SA
Case1 : from Core Cell
Case2 : from Core Cell
Case1 : from RED Cell
Case2 : from RED Cell

FIG. 8


REDMUX(15:0)
20
Redundancy Controller
DISINC
22
I/O Address Checker
UA(6:5)
CAM(6:5)
CAMIO(3:0)
CAMIO(3,2,1,0)=(1,1,1,1) =(15)10 ··· I/O15
CAM(6:5)=(1,0)
Inhibit I/O Increment
I/O
I/O#
UA
UA(6:5)
SA
CAM(6:5)
CAMIO(3:0)
REDMUX(15:0)
14
15
(0,0)
(0,1)
(1,0)
(1,1)
(1,0)
15
L
H

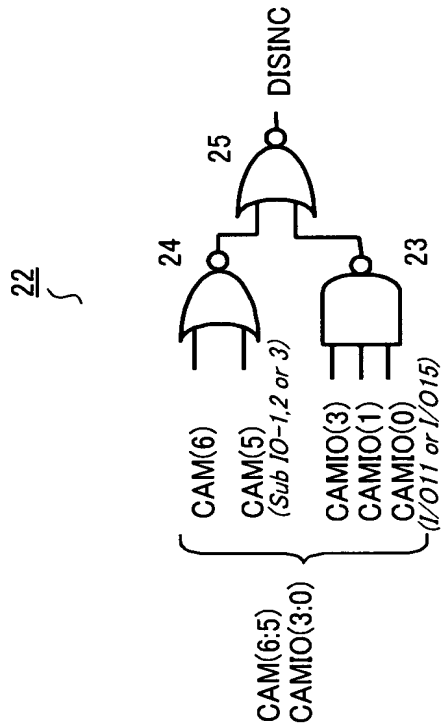

22
24
25
23
DISINC
CAM(6)
CAM(5)
(Sub IO-1,2 or 3)
CAMIO(3)
CAMIO(1)
CAMIO(0)
(I/O11 or I/O15)
CAM(6:5)
CAMIO(3:0)
I/O Address Checker Circuit

FIG. 9

Title: Semiconductor Memory Enabling Correct Substitution of Redundant Cell Array
Inventor: Andy CHEUNG
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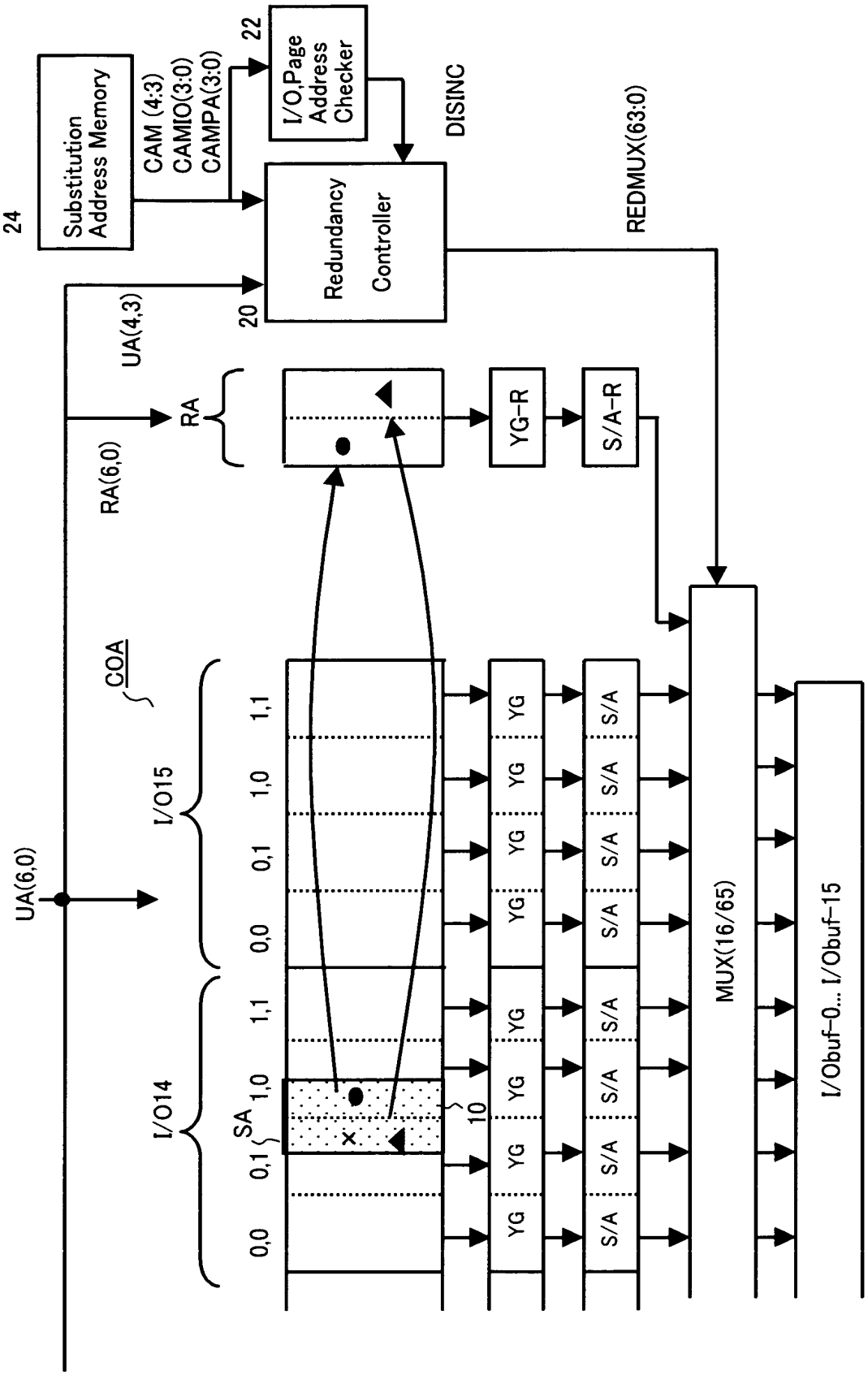
FIG. 10



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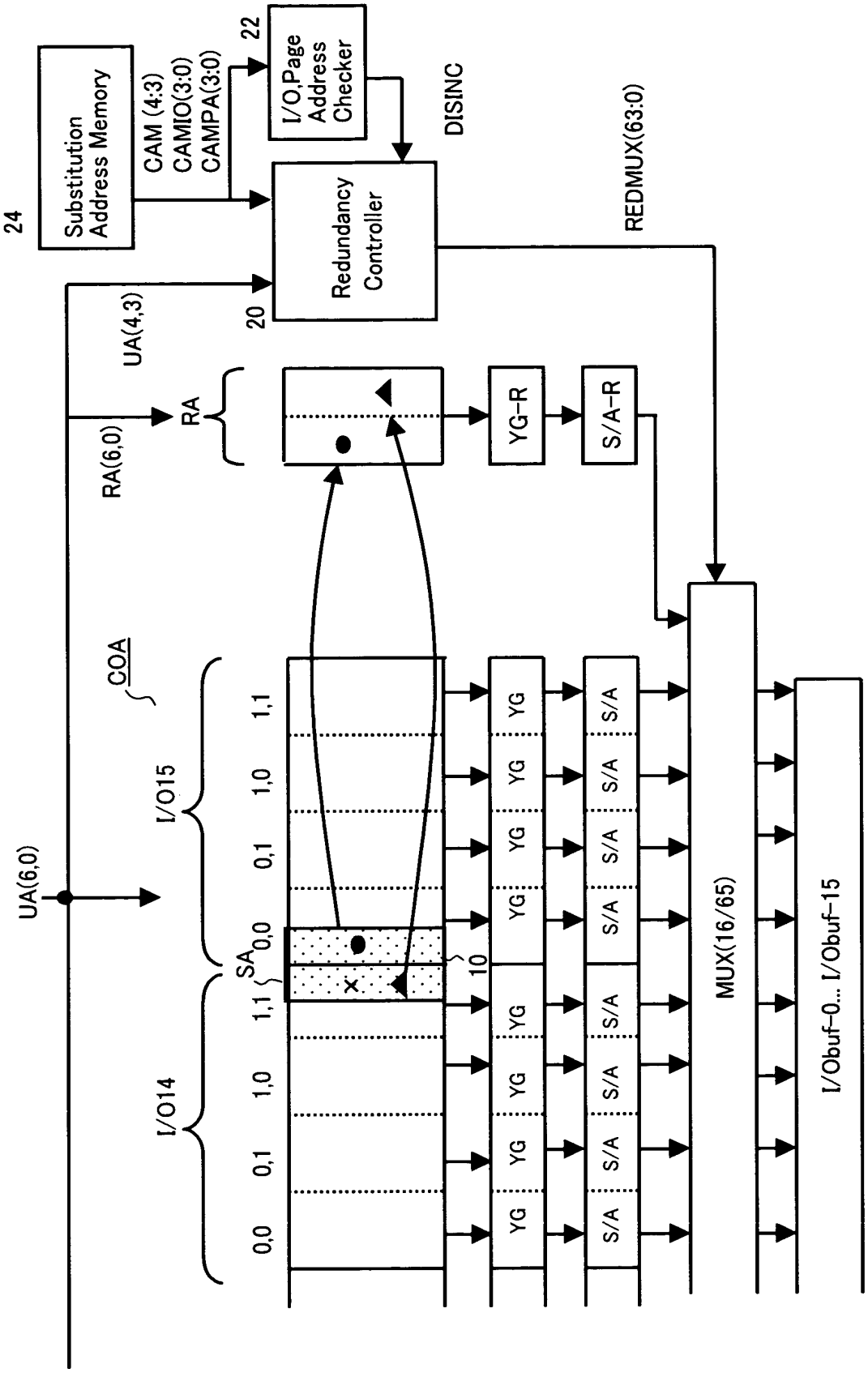
Appln. No. : New Application
Docket No.: 108066-00101

FIG. 11



Title: Semiconductor Memory Enabling Correct Substitution of Redundant Cell Array
Inventor: Andy CHEUNG
Appln. No. : New Application
Docket No.: 108066-00101

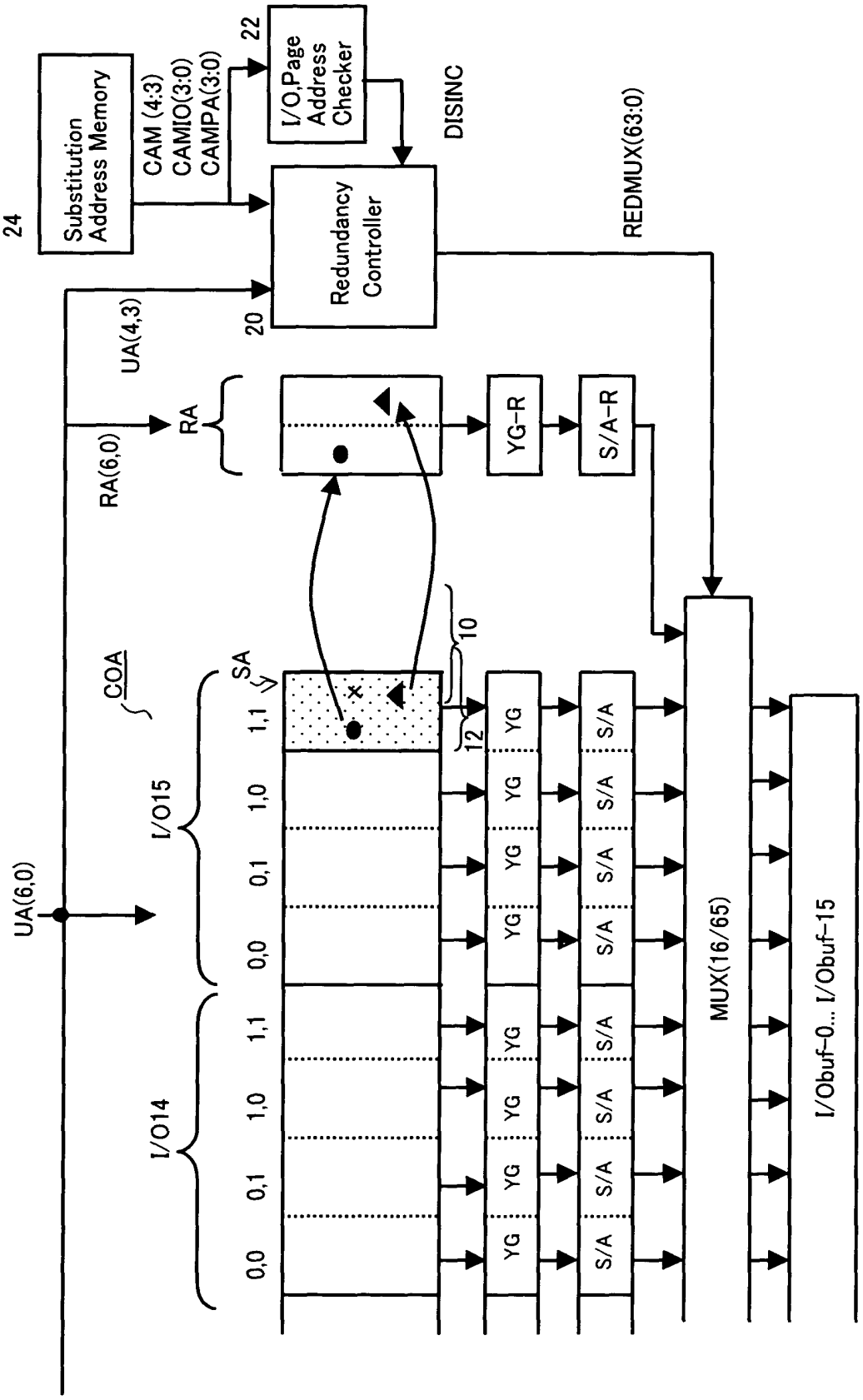


FIG. 12

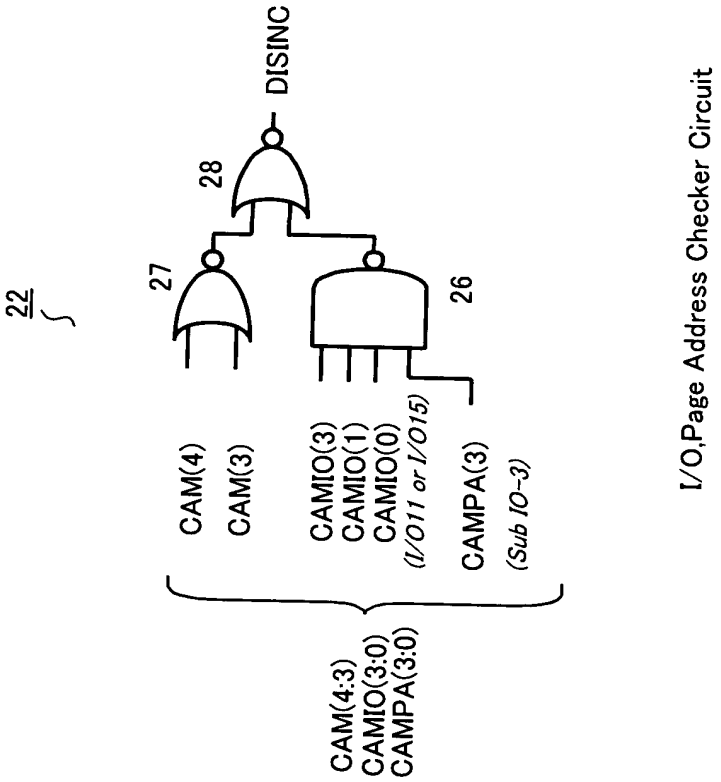

22
27
28
DISINC
26
CAM(4)
CAM(3)
CAMIO(3)
CAMIO(1)
CAMIO(0)
(I/O11 or I/O15)
CAMPA(3)
(Sub IO-3)
CAM(4:3)
CAMIO(3:0)
CAMPA(3:0)
I/O,Page Address Checker Circuit

FIG. 13